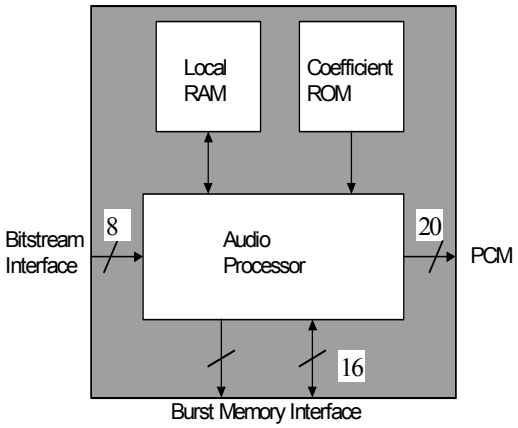
Jacobs Pineda, Inc. J1

AC-3/MPEG AUDIO DECODING CORE

FEATURES

- Decodes 5.1 Dolby AC-3 (ATSC A/52)
- Decodes MPEG layers 1 & 2 (ISO11172)
- Bitrates up to 640 KBPS
- 20 bit stereo PCM output
- Dolby Group A conformance.
- Support for DVD and SPDIF
- Supports DRAM sharing
- Low cost three block architecture
- Downmixes to Normal/Pro-Logic Stereo



PRODUCT DESCRIPTION

The J1 is a core cell design of an application specific signal processor which performs both Dolby AC-3 and MPEG audio decompression in a single design. The J1 is capable of decoding all AC-3 bitstreams with full support for bitstreams encoded with 5.1 channels and data rates of up to 640kb/s. The J1 downmixing capability produces stereo output in either normal or Pro-Logic compatible modes, making it ideal for DVD and set-top applications. For MPEG operation, J1 produces stereo output from either MPEG-1 or MPEG-2 audio bitstreams. The J1 audio quality meets the highest standards, allowing it to be used for the most demanding audio applications. The 20-bit PCM output yields Dolby "Group A" performance for AC-3, and conforms to the highest audio quality level specified by ISO11172-4 for MPEG bitstreams.

BURST MEMORY INTERFACE

In order to achive the lowest incremental cost for audio decoding, J1 has been designed for efficient integration with other functions, like MPEG video decoding or PC graphics controller functions. This level of integration is enabled by J1's glueless burst memory interface which allows the J1 to piggy back onto an internal memory bus and efficiently share DRAM memory with other functions. DRAM sharing allows on-chip RAM to be reduced by a factor of ten from what would otherwise be requried for the AC-3 and MPEG algorithms, thus minimizing cost. The burst memory interface is glueless, providing all memory addresses, and can be connected directly to a high speed memory bus without additional buffering. For efficient operation, all memory accesses are in blocks of 32 bytes, and J1 can tolerate latency inherent in shared memory systems. For non-integrated applications, the burst memory interface can be configured to directly address an on-chip SRAM.

SYSTEM FEATURES

Additional features are provided to support a wide variety of applications. For applications incorporating video, the J1 synchronization interface performs functions necessary for A/V synchronization with MPEG time stamps. For applications in automobiles or other noisy environments, the J1 core implements a dynamic range compression function which is compatible with Dolby Laboratories specifications. The J1 also provides stereo outputs which are ProLogic compatible. For DVD applications, the J1 provides PCM mode processing; with left, right, left+right (mono), volume control, and pass through modes. The J1 core also performs AC-3/MPEG framing necessary for interfacing to S/PDIF equipped external decoding devices. An

REV. A 2 Jan 2003

optional output module provides the single wire S/PDIF serial output. Other optional serial interface modules are available for I2C and 3-wire protocols.

SILICON COST

The complete dual-standard J1 core is only 16-20K gates in size, and including ROM and RAM, requires a silicon area of less than $2mm^2$ in a 0.25u CMOS processes. While other designs incorporate multiple logic, RAM, and ROM blocks for various functions, the J1 uses only three blocks, one logic, one RAM, and one ROM, thereby minimizing inter-block routing overhead and silicon area. Because RAM is unified into a single block, the J1 is able to employ overlay techniques to reuse the RAM for multiple purposes, thus minimizing the number of bytes needed, and further reducing the silicon area. The J1 design incorporates all buffering and interface logic, so that it may be used in a wide variety of applications with no additional logic or buffering.

DESIGN KIT

The J1 design kit is compatible with Synopsys and Verilog design methodology. J1 requires 0.35 micron or better technology, and is designed for synthesis with off-the-shelf gate array or standard cell ASIC libraries.

ANALOG OUTPUT

By combining the J1 core with the Jacobs Pineda, Inc. JDA1 DAC/PLL core, a complete audio decoding subsystem can be built for DVD applications, accepting AC-3/MPEG digital audio in, and producing analog and SPDIF outputs with a single clock source.

Functional Specifications

AC-3

- Coding standard: ATSC A/52
- Sampling rates: 48 kHz, 44.1 kHz, 32 kHz
- Coding modes: 1+1, 1/0, 2/0, 3/0, 2/1, 3/1, 2/2, 3/2
- Multi-channel down-mixing
- Re-matrixing to preserve Dolby Prologic encoding
- Conformance: Group A (20 bit)

MPEG

- Coding standard: ISO11172-3, layers 1,2
- Sampling rates: 48 kHz, 44.1 kHz, 32 kHz
- Conformance: Highest level (16 bit)

PCM

- PCM modes for non-compressed audio data
- Sampling rates: 48 kHz, 44.1 kHz, 32 kHz
- I/O: 16-24 bit input PCM, 16-bit output PCM
- Modes: PCM pass, Mono, Mono-L, Mono-R
- Other mixing functions possible. All scale by PCM scale factor.

SPDIF

- Frames compressed MPEG or AC-3 data into SPDIF stream.
- Standards: ATSC/A52 Annex B. , IEC 1967

CLOCK FREQUENCY

The J1 is designed to operate with a master clock rate of at least 54MHz.

Jacobs Pineda, Inc. 6280 Acacia Ave., Oakland, CA 94618, TEL: +1.415.641.9194, http://www.jacobspineda.com

AC-3/MPEG AUDIO DECODING CORE

DESIGN FLOW

The JPI design kit includes everything the customer needs to design the JPI core cell into their system ASIC. The design kit includes the core cell in Verilog netlist form, and verification tools consisting of a Verilog regression test bench, an executable for a bit-acurate simulator, and regression test vectors.

Synthesis

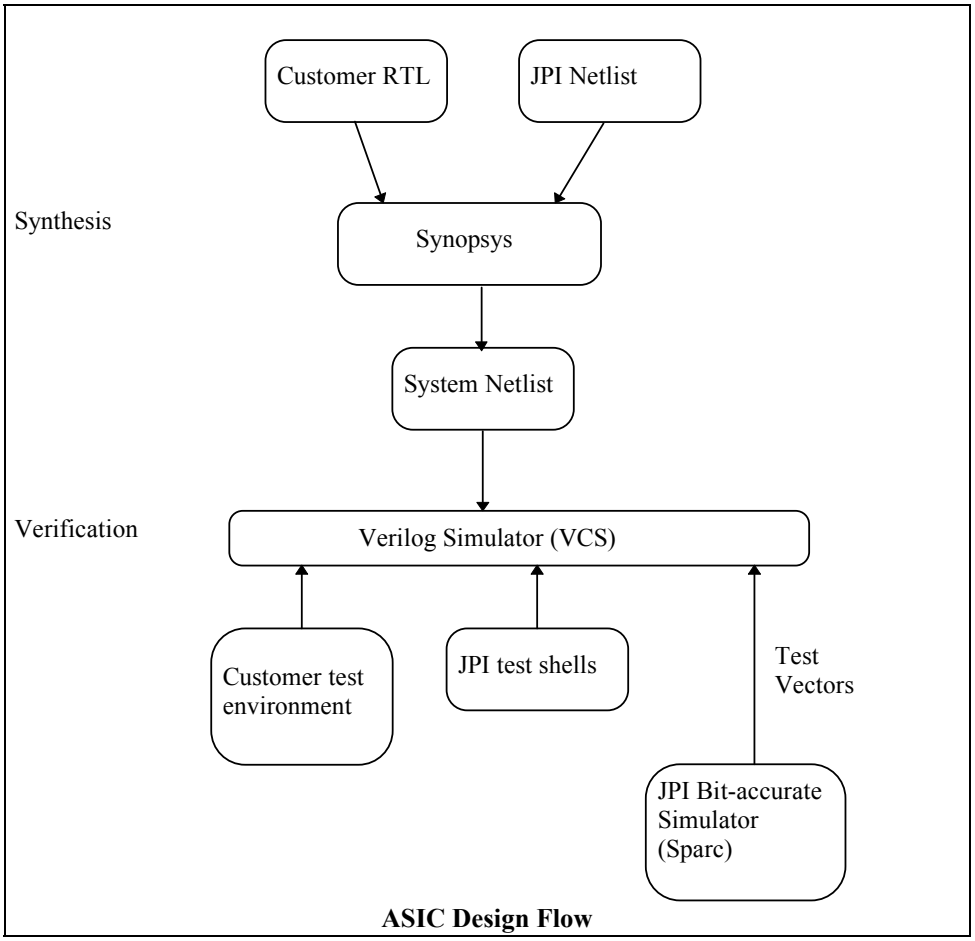
The J1 design kit is compatible with Synopsys Design Compiler. The customer supplies 0.35 micron (or better) Synopsys and Verilog libraries for the target technology. JPI synthesizes the core cell to the target techology and gives customer the core cell in netlist form.

The customer combines the JPI core cell netlist with their RTL to synthesize an entire ASIC.

Verification

The regression test shell, bit-acurate simulator, and regression test vectors allow the customer to verify the operation of the J1 core in isolation. In addition, the shells may be adapted for use in the customer's system level environment, allowing the J1 core to be tested in the system environment. The regression test scripts are configured for the Chronologics VCS Verilog simulator.

To support faster simulation, Synopsys VMC models may be provided under special arrangements with JPI.



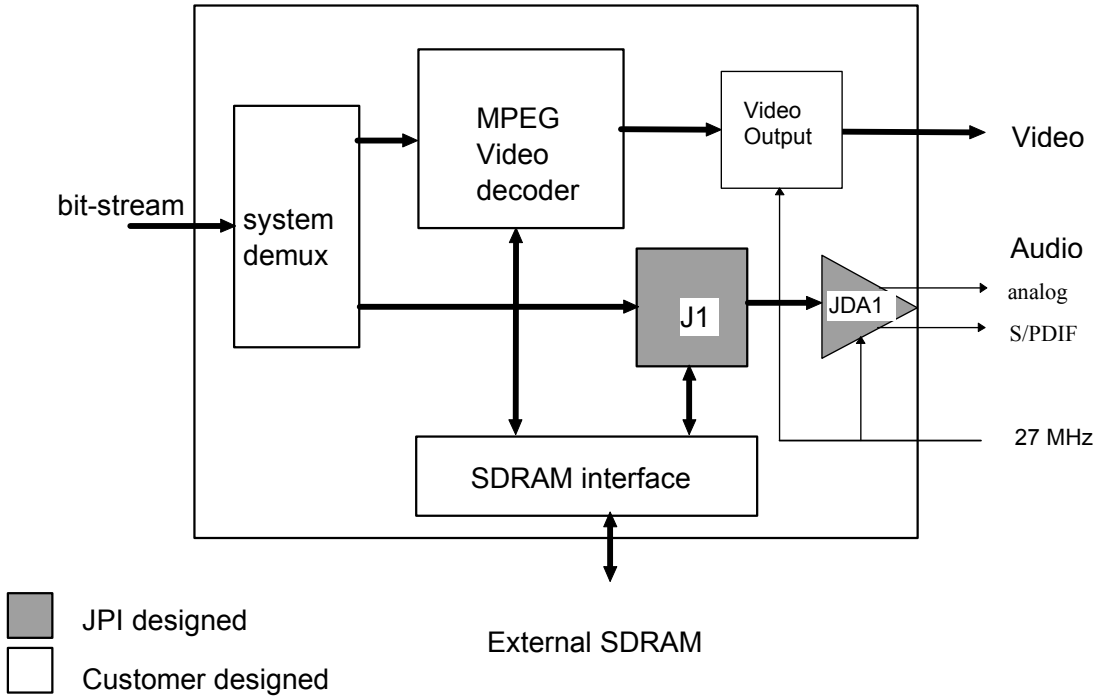
ASIC Design Flow

Jacobs Pineda, Inc. 6280 Acacia Ave., Oakland, CA 94618, TEL: +1.415.641.9194, http://www.jacobspineda.com

AC-3/MPEG AUDIO DECODING CORE

APPLICATIONS

The following diagram shows how the Jacobs Pineda, Inc. J1 and JDA1 core cells can be used to add MPEG/AC-3 audio decoding with analog output to an MPEG video decoder IC. In this application J1 interfaces directly to the shared SDRAM interface in order to minimize on-chip RAM. Further the JDA1 is clocked by the same 27MHz clock that clocks the video output circuitry.



INFORMATION:

For more information on the J1, contact Jacobs Pineda, Inc. at *info@jacobspineda.com.*

About Jacobs Pineda, Inc.

JPI is a design firm specializing in high volume, low cost, consumer audio IC designs. Its designs are licensed and employed by semiconductor and system manufacturers of audio solutions for the consumer and computing markets. Founded in 1995, JPI is a California Corporation with offices in Oakland. More information can be obtained on their web site at **http://www.jacobspineda.com.**