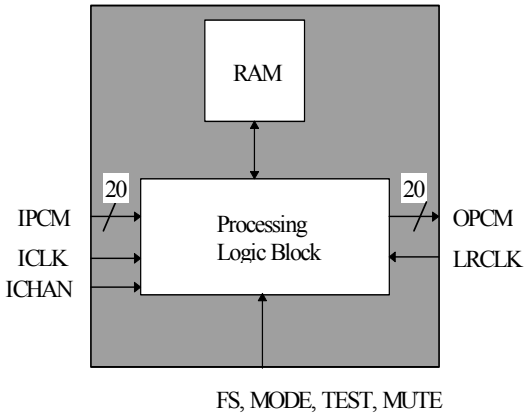
Jacobs Pineda, Inc. J5

TRUSURROUND®/SRS3-D® AUDIO PROCESSOR CORE

FEATURES

- Implements SRS Labs Trusurround™ 3-D
- Implements SRS Labs SRS 3D® also
- 6,4(Pro-Logic), or 2(stereo) channel PCM In
- 20 bit stereo PCM output
- Selectable Passive Matrix decoder
- Bypass passthrough/downmix modes
- High perfornamce datapath
- Low cost two block architecture
- Full Test mode capabilities for SRS testing
- Pre-certified performance by SRS Labs, Inc.
- 32kHz, 44.1kHz, and 48kHz sample rates



PRODUCT DESCRIPTION

The J5 is a digital VLSI core cell design of an application specific signal processor that performs both Trusurround™ and SRS 3-D® audio "virtualization" processing in a single design. The 3-D processing allows users to enjoy benefits of a multi-channel sound source with only two reproduction channels. For Dolby Digital® (AC-3) sources, the J5 accepts full 6-channel PCM inputs and performs the 3-D processing to produce output Left/Right signals. Similarly, for decoded ProLogic™ sources, the J5 accepts a 4-channel PCM input (L,C,R,S) and produces the same stereo output. When played through a conventional stereo sound system the user experiences "virtualized" multi-channel sound, as if the reproduction system was playing all 4 or 6 channels. In SRS 3-D mode, the J5 accepts a stereo PCM input and implements the SRS Labs 3-D algorithm to further spatialize the signal. The J5 downmixing capability produces stereo output in bypass mode. There is also a simple LR bypass mode which simply passes L/R inputs to the outputs. Of course, muting is also selectable. The J5 audio quality meets the highest standards, allowing it to be used for the most demanding audio applications. The 24-bit PCM output yields a high level of compilance with the SRS specifications for Trusurround by minimizing quantization error. High precision is maintained internal to the J5.

ECONOMICAL VLSI CORE CELL

In order to achive the lowest incremental cost for 3-D audio processing, the J5 has been designed for efficient integration with other functions, like Dolby Digital® audio decoding and D/A converters. Processing is performed entirely in the digital domain, and the J5 is made up of a single logic block and small local RAM, to minimize interblock routing requirements.

The complete dual-standard J5 core is only 3K gates in size, and including its RAM, requires a silicon area of approximately 0.3mm^2 in a typical 0.25u CMOS process. The J5 design incorporates all buffering and interface logic, so that it may be used in a wide variety of applications with no additional logic or buffering.

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3-D AUDIO PROCESSOR CORE

FULL TEST CAPABILITIES

For ease in testing and certification, the J5 has a flexible test/control interface. This allows the J5 to isolate any of its inputs and outputs via muting and to selectively disable internal signal paths to allow for testing the individual filtering and gain responses that make up the 3-D processing. This allows a set of tests to be performed exactly as specified in the SRS Labs Trusurround Specificatons. The J5 bit-accurate performance of the core cell design kit has been granted a Pre-certification approval by SRS Labs, Inc.

INPUT/OUTPUT INTERFACE

Inputs and outputs are fully double buffered allowing flexible interface specifications. Parallel interfaces allow easy interconnection with other digital audio cells in a VLSI. Typically, a standard serial I^2S/EIAJ 3-wire interface is used.

SYSTEM FEATURES

An optional output module provides the single wire S/PDIF serial output. Other optional serial interface modules are available for I^2C and 3-wire protocols.

CLOCK FREQUENCY

The J5 is designed to operate with a master clock rate of at least 12MHz, although clock rates of 54MHz or higher can be used if different clock rates are more desirable in a specific application. The J5 is typically synthesized to 27MHz - the System Time Clock (STC) for MPEG-based audio/video systems.

DESIGN KIT

The J5 design kit is compatible with Synopsys and Verilog design methodology. J5 requires 0.35 micron or better technology, and is designed for synthesis with off-the-shelf gate array or standard cell ASIC libraries.

Functional Specifications

SRS Trusurround™

- Conforms to SRS Labs Trusurround Specifications.
- Sampling rates: 48 kHz, 44.1 kHz, 32 kHz
- 4 or 6-channel input (Prologic compatible)
- Optional Passive Matrix decoding for ProLogic encoded stereo inputs
- Conformance: Highest Level (16-bit)

SRS 3-D®

- Conforms to SRS Labs Trusurround Specifications in SRS 3D mode.
- Sampling rates: 48 kHz, 44.1 kHz, 32 kHz
- 2-channel input/output
- Conformance: Highest level (16 bit)

Matrix Decoding

- Allows stereo Prologic™ encoded input to be passive matrix decoded to 4-channels using simple sum/difference matrix.
- Resulting 4 channel output is then Trusurround processed.

Bypass Modes / Muting

- Performs *downmix* of 4/6 channel inputs to stereo outputs using simple matrix.
- Pass through mode: Left/Right Bypass
- I/O: Serial 16-24- bit input PCM (I^2S/EIAJ)
- Selectable muting on any input/output channel.

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3-D AUDIO PROCESSOR CORE

DESIGN FLOW

The JPI design kit includes everything needed to design the JPI core cell into their system ASIC. The design kit includes the core cell in Verilog netlist form, and verification tools consisting of a Verilog regression test bench, an executable for a bit-acurate simulator, regression test vectors, and a complete J5 interface specification..

Synthesis

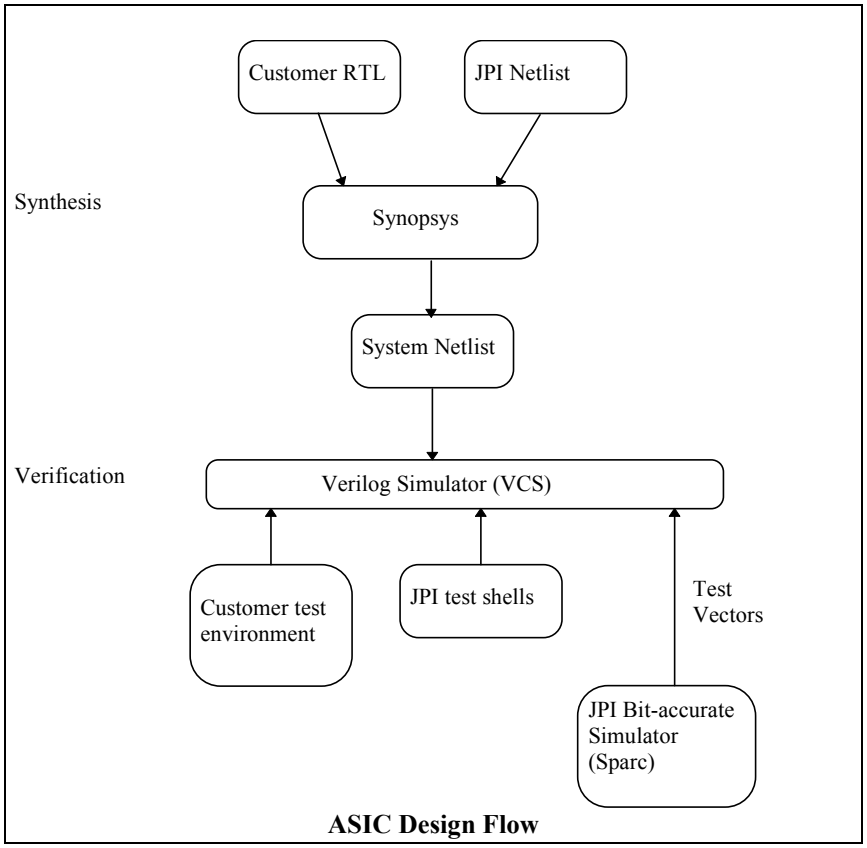
The J5 design kit is compatible with Synopsys Design Compiler. The customer supplies 0.35 micron (or better) Synopsys and Verilog libraries for the target technology. JPI synthesizes the core cell to the target techology and gives customer the core cell in netlist form.

The customer combines the JPI core cell netlist with their RTL to synthesize an entire ASIC.

Verification

The regression test shell, bit-acurate simulator, and regression test vectors allow the customer to verify the operation of the J5 core in isolation. In addition, the shells may be adapted for use in the customer's system level environment, allowing the J5 core to be tested in the system environment. The regression test scripts are configured for the Chronologics VCS Verilog simulator.

To support faster simulation, Synopsys VMC models may be provided under special arrangements with JPI.



ASIC Design Flow

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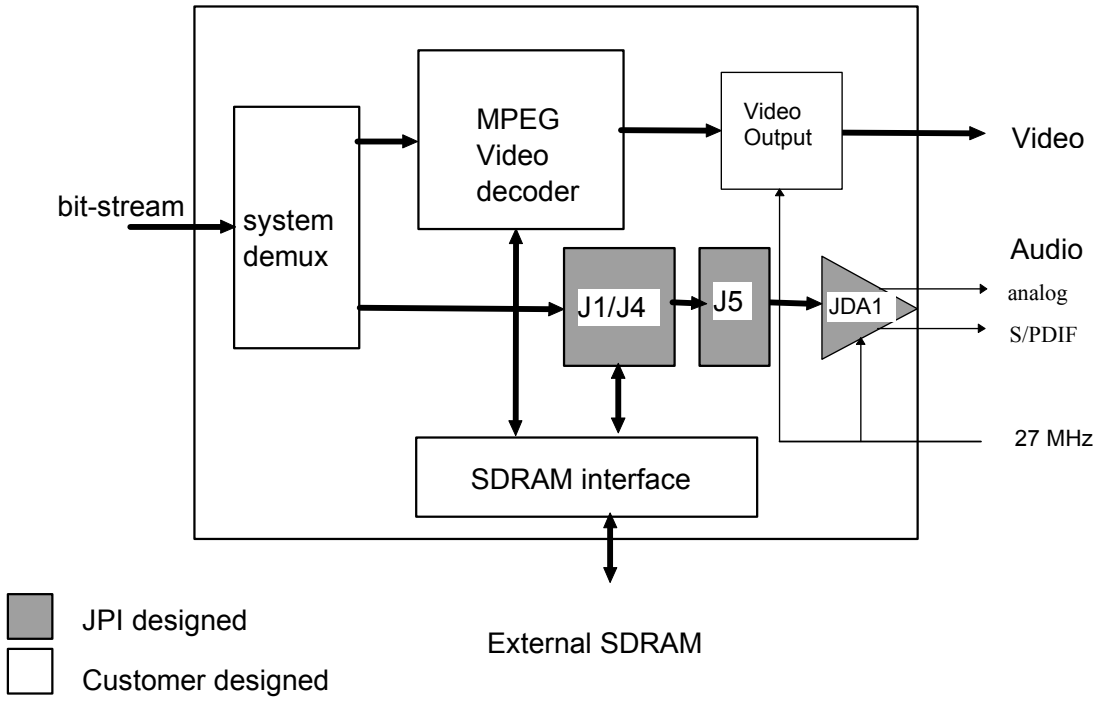
APPLICATIONS

By combining the J5 core with other Jacobs Pineda, Inc. core cells, the **JDA1** DAC/PLL core as an output device, and the **J1/J4** Dolby Digital/MPEG Audio Decoder core cell, a complete audio decoding subsystem can be built for DVD applications, accepting AC-3/MPEG digital audio in, and producing 3-D analog and SPDIF outputs with a single clock source.

The following diagram shows how the Jacobs Pineda, Inc. J1/J4 and JDA1 core cells can be used to add MPEG/AC-3 audio decoding with analog output to an MPEG video decoder IC. In this application J1/J4 interfaces directly to the shared SDRAM interface in order to minimize on-chip RAM. Further, the JDA1and J5 are clocked by the same 27MHz clock that clocks the video output circuitry, providing a "3-D" DAC virtualized stereo output.



INFORMATION:

For more information on the J5, visit our web page at ***http://www.jacobspineda.com*** or contact Jacobs Pineda, Inc. by Email at ***info@jacobspineda.com***.

About Jacobs Pineda, Inc.

JPI is a design firm specializing in high volume, low cost, consumer audio IC designs. Its designs are licensed and employed by semiconductor and system manufacturers of audio solutions for the consumer and computing markets. Founded in 1995, JPI is a California Corporation with offices in Oakland. More information can be obtained on their web site at **http://www.jacobspineda.com.**