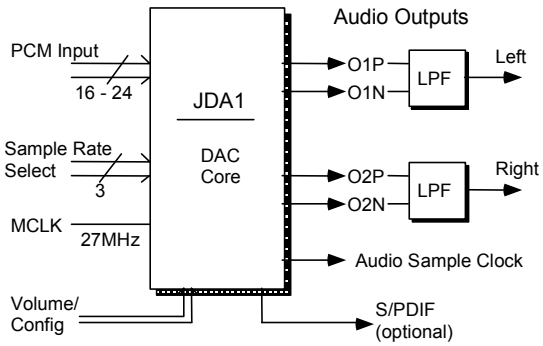
MULTI-RATE AUDIO DAC/PLL
16-BIT/18-BIT/20-BIT/24-BIT

FEATURES

- Operates from **single 27/54MHz clock**.
- Ideal for **MPEG/AC3** based systems
- Generates all common audio sample clocks from 27/54MHz master clock
- High Performance >16 bit resolution
- Accepts 16-24 bit PCM inputs
- 95dB integrated Volume control in 1dB steps
- Many muting options including soft-mute, auto-mute, etc.
- **96kHz** operation w/54MHz master clock



PRODUCT DESCRIPTION

The JDA1 is a digital-to-analog converter core cell suitable for all high quality audio multimedia applications. The JDA1 accepts a stereo digital PCM input signal at a standard sample rate (up to 24-bit resolution), and produces stereo analog outputs from that signal using a single master 27MHz clock, the same frequency as the system time clock (**STC**) of MPEG based systems. The baseline JDA1 is a fully digital Sigma-Delta converter that produces a pulsed output, which works in conjunction with a simple off-chip analog filter to provide the analog outputs. The JDA1 is applicable to switched-capacitor output filter circuitry as well, however the baseline configuration is most applicable to large digital VLSI applications requiring audio outputs.

The JDA1 contains three main processing blocks. The first is an interpolation filter engine, which increases the sample rate of the input PCM signal to 8fs, providing approximately 65dB of image rejection.

The second block performs noise-shaping and pulse shaping. The third block is a Phase-Lock Loop (PLL) to derive timing from the master clock.

A standard 3-wire serial PCM input interface allows I^2S/EIAJ 24-bit digital audio signals to be fed to the JDA1. An S/PDIF transmitter allows formatting the input stereo PCM samples into the single-wire format used to send digital audio signals between audio products. This is programmable, allowing the sending of compressed data also, as specified by Dolby Labs for AC-3 signals. Finally, simple 3-wire or I^2C microprocessor interfaces are available for allowing the setting of volume, muting, and other configuration bits inside the JDA1 from a host processor.

The JDA1 is very efficient in silicon area, requiring only approximately $0.5mm^2$ in a standard 0.18u CMOS process. This includes logic gates and RAM necessary for the signal processing. No custom cell libraries are required. For ease in floorplanning, the JDA1 consists of only a single logic block plus one 1-port RAM. The JDA1 follows the Verilog/Synopsys design flow for easy porting to new libraries.

For 96kHz applications, the JDA1 may be clocked at 54MHz. In this mode, the supported sample rates are 32, 44.1, 48, and 96kHz.

REV. B 25 Jan 2003

MULTI-RATE AUDIO DAC/PLL
16-BIT/18-BIT/20-BIT/24-BIT

APPLICATIONS

The JDA1 DAC is suitable for digital audio VLSI applications that operate at audio sampling rates of 32 kHz, 44.056 kHz, 44.1 kHz and 48kHz and require analog outputs. The JDA1 produces stereo outputs from a standard 2-channel digital input. Its built in PCM serial interface allows the JDA1 to accept PCM digital audio in a variety of serial formats such as Philips I^2S or EIAJ 16 to 24 bit right justified. An optional digital output module supplies data in S/PDIF format.

Control of the JDA1 operating modes and features, such as volume control and muting, are handled by a control bus input. This may be driven by optional host interfaces. In a typical VLSI application, there is usually a single host interface that supplies all of the modules on the IC, and the JDA1 can simply act as a client of this interface.

The oversampled output is differential and requires one external op amp filter/buffer to generate a single ended audio output. Analog filter rolloff at 20 kHz is compensated by the internal digital filters.

A low-jitter, crystal-based system clock at 27MHz is required; all audio clocks needed by the DAC are derived internally from this system clock. The incorporation of an integrated Phase Lock Loop (PLL) with D/A conversion(DAC) enables the JDA1 to support multiple audio sample rates from a single 27MHz input clock frequency. This eliminates the expense of audio clock generation circuitry required for MPEG and other multi-sample-rate applications. Optionally, the JDA1 may operate with a single 54MHz clock, to support the 96kHz sample rate.

AUDIO CLOCK GENERATION

The JDA1 PLL circuit has several modes of operation. In *master* mode, the JDA1 will derive internally the audio sample clock directly from the 27MHz master clock, and supply this as an output to prompt for data from a digital audio source. In *slave* mode, the JDA1 locks onto an external audio sample clock(e.g. from an S/PDIF receiver), to phase lock with a digital audio source that derives its own clocks. The JDA1 also supplies multiples of the audio sample rate clock at *fs*. A 128x and 256x output are supplied for external circuits such as an S/PDIF formatter. These outputs may be divided down to form the audio clock at *fs*, since the JDA1 can track the phase of any input audio clock.

AUDIO PERFORMANCE

Audio performance measurements were taken on a stand-alone application of the JDA1. The test conditions are listed in Table 2. Similar performance has been measured on VLSI applications of the JDA1, including digital ICs with over 250K gates. All filters used are internal to the Audio Precision analyzer, with the exception of an external 20 kHz brickwall lowpass filter used for measuring Dynamic Range and THD+N vs. Amplitude. A summary of the audio performance is given in Table 3.

TEST RESULTS SUMMARY

The frequency response is extremely flat throughout the audio band; rolloff at 20 kHz is virtually nonexistent. Passband ripple, amplitude imbalance, and phase imbalance are all negligible.

The THD+N at 1 kHz is better than -90dBFS (dB w.r.t. full scale) (.003%) when measured with the external 20 kHz brickwall lowpass filter. The THD+N at -60 dBFS is -33.8 dB with 16 bit data, improving to -37.9 dB with 18 bit data. The calculated dynamic ranges are 93.8 dB and 97.9 dB, respectively (dithered input signals). The THD+N versus frequuency remains below -88dBFS over the entire 20kHz audio bandwidth. Signal to noise ratio at digital silence exceeds 100 dB. Crosstalk is nearly -120 dB at 1 kHz and rises to -92 dB at 20 kHz (a function of PC board layout).

TECHNOLOGY COMPATIBILITY

An great advantage of the JDA1 architecture is that it consists of entirely digital signal processing circuitry and as such, it is compatible with other digital circuitry and integrated circuit processes. Sigma-delta converters such as the JDA1 are by nature mostly digital. Figure 1 shows a typical sigma-delta stand-alone DAC, which consists of

the digital processing circuitry to raise the sample rate and perform noise shaping. Following this, most manufacturers exploit sampled-data switched-capacitor filtering to attenuate the high frequency noise of the oversampled signal and provide a purely analog signal output. This configuration has the advantage of the highest degree of integration. However, it also has a disadvantage that the process technology is constrained be "analog MOS", or a process with 2 poly layers for constructing the capacitors required. Processes geared towards mixed-signal functions typically lag those for all-digital VLSI in design rules, and they are usually NOT offered by ASIC vendors.

The JDA1 architecture is suitable for integration of switched capacitor output filtering as well, however its baseline design uses a pulse density modulation output to provide digitally shaped output pulses that may be filtered to recover the baseband audio with off-chip circuitry. The requirement for the external off-chip filter looks to be a disadvantage over the completely integrated solution. However, looking at Figure 1 again, one can see why this partitioning makes sense for large VLSI applications.In a multi-media system, there may be a very high level of integration of all of the digital functions as shown, where a video decoder, audio decoder, memory interface, host interface, video encoder and DAC are all integrated on a single VLSI. In this case, there would be a great disadvantage in requiring a special process technology such as 2-poly for the entire IC, when only a small percentage of the silicon area requires analog circuitry. Manufacturers would need to employ the latest technologies available to make the IC cost and power-consumption feasible. Note also that such IC technologies are all at 3.3V power supply, which further stresses the design of analog low-noise circuitry.

The JDA1 pulse density output can be filtered by a simple single-stage filter. The filter is off-chip, but it also acts as a buffer/driver between the expensive large VLSI chip and the outside world. Often times, product designs employ such buffers in any case, to implement a final analog muting function or more drive capability. Only several inexpensive capacitors are needed to convert a buffer of this sort to the required reconstruction filter for the JDA1. The isolation is important to prevent damage to the large VLSI by user errors

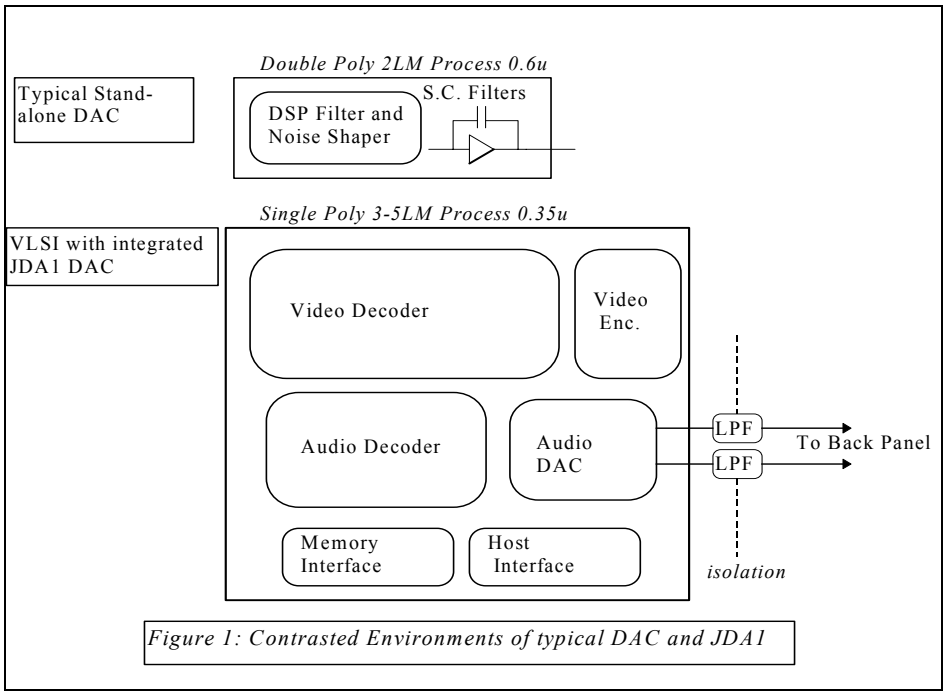


Figure 1: Contrasted Environments of typical DAC and JDA1

in hookup.

For these reasons, the JDA1 baseline architecture fits well for large integrated digital system design.

One other design tradeoff in the pulse density output is the sensitivity to clock jitter, which has the effect of modulating the output amplitude by affecting the width of the output pulses. The JDA1 output pulses are clocked by a separate clock input, which must be tied to a crystal-derived 27MHz or 13.5MHz time base to maintain the audio quality. For this reason, the JDA1 is targeted towards MPEG-based systems, where a high quality VCXO derived 27MHz time base is already required.

Audio Sample Rate Capabilities:

The JDA1 is designed to support 7 audio sample rates. These sample rates are shown in Table 1 along with the appropriate divisors to use in generating the respective 256fs rate clocks from the 27 MHz source. For a 54MHz master clock, all sample rates below are doubled, allowing **96kHz** operation.

TABLE 1. JDA1 Supported Audio Sample Rates (27MHz, *rates doubled for 54MHz clock*)

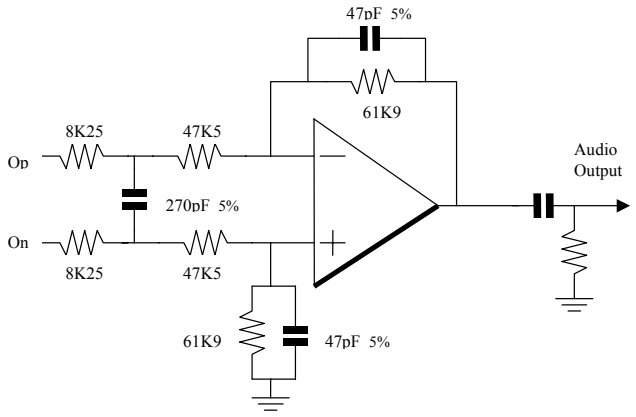
Mode	Sample Rate (fs)	Timebase (T)	Divisor (M)	T/M = 256fs
DVD	48 KHz	27 MHz	1125/512	12.2880 MHz
CD	44.1 KHz	27 MHz	1875/784	11.2896 MHz
TV	44.056 KHz	27 MHz	2145/896	11.2783 MHz
Lo-Fi	32 KHz	27 MHz	3375/1024	8.1920 MHz
MPEG Half-rate	24kHz	27MHz	3375/2048	6.144MHz
MPEG Half-rate	22.05kHz	27MHz	1875/1568	5.6488MHz
MPEG Half-rate	16kHz	27MHz	3375/2048	4.096kHz

The JDA1 may be customized to other sample rates upon request.

MEASUREMENT OUTPUT LOWPASS FILTER

The circuit below shows the output interface needed to implement the analog output anti-aliasing filtering function for each channel. It was used to take the measurements shown in this datasheet.

Figure 2. Output Audio Analog Filter Circuit Implementation for consumer applications



TEST CONDITIONS FOR JDA1 MEASURED PERFORMANCE

Table 2 - Test Conditions (unless otherwise specified)

Parameter	Frequency	Amplitude	Filter
Output Level	1 kHz	0 dBFS	
Amplitude vs. Frequency	.02-20 kHz	0 dBFS	
L/R Amplitude Imbalance	.02-20 kHz	0 dBFS	
L/R Phase Imbalance	.02-20 kHz	0 dBFS	
Total Harmonic Distortion + Noise (THD+N) at 1kHz	1 kHz	0 dBFS	22 kHz LPF
(THD+N) vs. Freq.	.02-20 kHz	0 dBFS	20 kHz LPF (external)
Total Harmonic Distortion + Noise (THD+N) vs. Ampli.	1 kHz	0-80 dBFS	20 kHz LPF (external)
Dynamic Range	1 kHz	-60 dBFS	20 kHz LPF (external)
IMD (CCIF 400 Hz & 4080 Hz)	80 Hz	0 dBFS	80 Hz BPF
L/R Crosstalk (Isolation)	.02-20 kHz	0 dBFS	BPF at Fundamental
Signal to Noise Ratio (SNR) (Digital Silence)	1 kHz	OFF	22 kHz LPF

Digital Audio Generator		FFT Analyzer Settings	
Data Length:	16 bits	Record Length:	16384
Data Format:	SPDIF	Averages:	16
Sampling Rate (Fs):	44.1 kHz	Filters:	20 kHz LPF (external)
Bit Clock	64*Fs	Windows:	Hann
System Clock:	27.0 MHz	Sampling Rate:	44.1 kHz
Dithering:	ON (Rectangular)	Trigger:	Auto

MEASURED AUDIO PERFORMANCE FIGURES

See Table 2 for test conditions.

Table 3 - JDA1 Typical Measured Audio Performance Vdd=5V

Parameter		Units	Measured Left Channel	Measured Right Channel
Output Level		Vrms	1.747 (1)	1.750
Amplitude vs. Frequency		dB, p-p	<0.15 (3)	<0.15
L/R Amplitude Imbalance		dB	< 0.1 (3)	n/a
L/R Phase Imbalance		degrees, p-p	<4 (3)	n/a
(THD+N)	at 1 kHz vs. Freq.	dB dB	-94.1 <-88	-92.1 <-88
(THD+N)	vs. Amplitude	dB	< -92	< -92
Dynamic Range	16 bit data 18 bit data	dB dB	93.8 (2) 97.9	93.9 98.2
IMD (CCIF 4000 Hz & 4080 Hz		dB	-99.5	-103.0
Crosstalk (Isolation):	1 kHz 20 kHz	dB dB	-117 -92	-117 -96
Signal to Noise Ration (SNR) (Digital Silence)		dB	100.3	100.3
Variation in SNR vs. Sample Rate		dB	< 1	< 1

Notes:

(1) For a 3.3V power supply or ASIC technology, the output level nominally drops to 1.16Vrms, but may be adjusted by the resistor values in the external filter/buffer stage.

(2) Dithering used. With no dithering, 16-bit data dynamic range increases approximately 3dB.

(3) Function of tolerance of external filter components. Typical shown with 1% R, 5% C. L/R Amplitude imbalance is nominally 0dB and L/R phase imbalance is nominally < 0.5 degrees prior to output filter.

DESIGN FLOW

The JPI design kit includes everything the customer needs to design the JPI core cell into their system ASIC. The design kit includes the core cell in Verilog netlist form, and verification tools consisting of a Verilog regression test bench, an executable for a bit-acurate simulator, and regression test vectors.

Synthesis

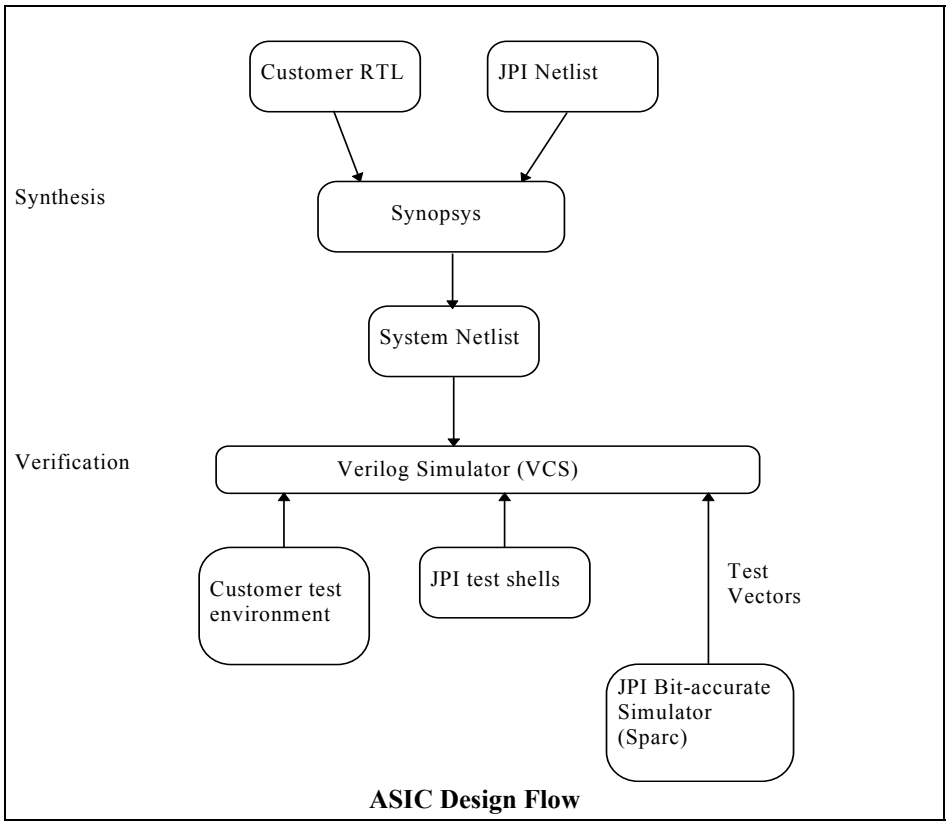
The J1 design kit is compatible with Synopsys Design Compiler. The customer supplies 0.35 micron (or better) Synopsys and Verilog libraries for the target technology. JPI synthesizes the core cell to the target techology and gives customer the core cell in netlist form.

The customer combines the JPI core cell netlist with their RTL to synthesize an entire ASIC.

Verification

The regression test shell, bit-acurate simulator, and regression test vectors allow the customer to verify the operation of the J1 core in isolation. In addition, the shells may be adapted for use in the customer's system level environment, allowing the J1 core to be tested in the system environment. The regression test scripts are configured for the Chronologics VCS Verilog simulator.

INFORMATION:
For more information on the JDA1, please contact Jacobs Pineda, Inc.at *info@jacobspineda.com.*



ASIC Design Flow